Notice of Allowability	Application No.	Applicant(s)	
	10/082,776	BENNETT ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 20 August 2007*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Steven Hanke (Reg. No. 58,076) on 22 October 2007.

3. The following amendments are demarked with the standard amendment notations, such as an identifier for the claims identifying whether it was amended, cancelled, etc.; strikethrough or double brackets for deleted text; and underline for added text. The application has been amended as follows:

a. Claim 1: (Currently Amended) A context switching system for a multi-thread execution pipeline loop having a pipeline latency, comprising:

i. A single miss fulfillment first-in-first-out buffer (FIFO);

ii. A context switch requesting subsystem configured to:

(1) Detect a device request from a <u>first</u> thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency, and

(2) Generate a context switch request for said <u>first</u> thread; and

iii. A context controller subsystem configured to receive said context switch request and, based thereon, store said <u>first</u> thread in said single miss fulfillment FIFO to prevent said <u>first</u> thread from executing until said

device request is fulfilled, said first thread sequencing entirely through ~~entire~~ said single miss fulfillment FIFO at a rate ~~substantially~~ equivalent to said pipeline latency before exiting therefrom.

b. Claim 2: (Currently Amended) The context switching system as recited in Claim 1 wherein said context controller subsystem is further configured to allow a new thread to enter said multi-thread execution pipeline loop after storing said first thread in said miss fulfillment FIFO.

c. Claim 3: (Currently Amended) The context switching system as recited in Claim 1 wherein said context controller subsystem is further configured to allow other threads within said multi-thread execution pipeline loop to continue to execute while said first thread is waiting for said device request to be fulfilled.

d. Claim 4: (Currently Amended) The context switching system as recited in Claim 1 wherein said context controller subsystem is further configured to:

i. Store said first thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop, and

ii. Reinsert said first thread into said multi-thread execution pipeline loop at a beginning position after said first thread exits said miss fulfillment FIFO.

e. Claim 5: (Currently Amended) The context switching system as recited in Claim 1 wherein said first thread is looped back to a beginning stage of said multi-thread execution pipeline loop when said first thread reaches an end stage of said multi-thread execution pipeline loop and said first thread has not finished processing.

f. Claim 6: (Cancelled)

g. Claim 7: (Original) The context switching system as recited in Claim 1 wherein said device request is a request to access external memory due to a cache miss status.

h. Claim 8: (Currently Amended) For use with a multi-thread execution pipeline loop having a pipeline latency, a method of operating a context switching system, comprising:

i. Detecting a device request from a first thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency;

ii. Generating a context switch request for said first thread when said first thread issues said device request; and

iii. Receiving said context switch request and storing said first thread based thereon in a single miss fulfillment first-in-first-out buffer (FIFO) until said device request is fulfilled, said first thread sequencing entirely through ~~entire~~ said single miss fulfillment FIFO at a rate ~~substantially~~ equivalent to said pipeline latency before exiting therefrom.

i. Claim 9: (Currently Amended) The method as recited in Claim 8 further comprising allowing a new thread to enter said multi-thread execution pipeline loop after storing said first thread in said miss fulfillment FIFO.

j. Claim 10: (Currently Amended) The method as recited in Claim 8 further comprising allowing other threads within said multi-thread execution pipeline

loop to continue to execute while said first thread is waiting for said device request to be fulfilled.

k. Claim 11: (Currently Amended) The method as recited in Claim 8 further comprising:

i. Storing said first thread in said miss fulfillment FIFO upon reaching an end position of said multithread execution pipeline loop, and

ii. Reinserting said first thread into said multi-thread execution pipeline loop at a beginning position after said first thread exits said miss fulfillment FIFO.

l. Claim 12: (Currently Amended) The method as recited in Claim 8 further comprising looping said first thread back to a beginning stage of said multi-thread execution pipeline loop when said first thread reaches an end stage of said multi-thread execution pipeline loop and said first thread has not finished processing.

m. Claim 13: (Cancelled)

n. Claim 14: (Original) The method as recited in Claim 8 wherein said device request is a request to access external memory due to a cache miss status.

o. Claim 15: (Currently Amended) A fast pattern processor that receives and processes protocol data units (PDUs), comprising:

i. A dynamic random access memory (DRAM) that contains instructions;

ii. A memory cache that caches certain of said instructions from said DRAM; and

iii. A tree engine that parses data within said PDUs and employs said DRAM and said memory cache to obtain ones of said instructions, including:

(1) A multi-thread execution pipeline loop having a pipeline latency, and

(2) A context switching system for said multi-thread execution pipeline loop, having:

(a) A single miss fulfillment first-in-first-out buffer (FIFO);

(b) A context switch requesting subsystem that:

(i) Detects a device request from a first thread executing within said multithread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency, and

(ii) Generates a context switch request for said first thread, and

(3) A context controller subsystem that receives said context switch request and, based thereon, stores said first thread in said single miss fulfillment FIFO until said device request is fulfilled, said first thread sequencing entirely through ~~entire~~ said single miss fulfillment FIFO at a rate ~~substantially~~ equivalent to having a said pipeline latency before exiting therefrom.

p. Claim 16: (Currently Amended) The fast pattern processor as recited in Claim 15 wherein said context controller subsystem further allows a new thread to enter said multi-thread execution pipeline loop after said first thread is stored in said FIFO.

q. Claim 17: (Currently Amended) The fast pattern processor as recited in Claim 15 wherein said context controller subsystem further allows other threads within said multi-thread execution pipeline loop to continue to execute while said first thread is waiting for said device request to be fulfilled.

r. Claim 18: (Currently Amended) The fast pattern processor as recited in Claim 15 wherein said context switching system is further configured to:

i. Store said first thread in said miss fulfillment FIFO upon reaching an end position of said multithread execution pipeline loop, and

ii. Reinsert said first thread into said multi-thread execution pipeline loop at a beginning position after said first thread exits said miss fulfillment FIFO.

s. Claim 19: (Currently Amended) The fast pattern processor as recited in Claim 15 wherein said first thread is looped back to a beginning stage of said multi-thread execution pipeline loop when said first thread reaches an end stage of said multi-thread execution pipeline loop and said first thread has not finished processing.

t. Claim 20: (Cancelled)

u. Claim 21: (Original) The fast pattern processor as recited in Claim 15 wherein said device is said DRAM and said device request is a request to access said DRAM due to a cache miss status from said memory cache.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: Independent claims 1, 8, and 15 recite limitations that, in combination, are not taught by the prior art searched and found. Specifically, the prior art searched and found has not taught the limitation "said first thread sequencing entirely through said single miss fulfillment FIFO at a rate equivalent to said pipeline latency before exiting therefrom" in combination with the other limitations.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

18 October 2007